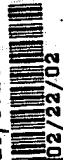


10/08/1491



U.S. UTILITY Patent Application

PATENT NUMBER and
ISSUE DATE

APPL NUM 10081491	FILING DATE 02/22/2002	CLASS 438	SUBCLASS 100	GAU 2812	EXAMINER Roman
**APPLICANTS: Pendse Rajendra; Ahmad Nazir; Chen Andrea; Kim Kyung-Moon; Kweon Young-Do; Tam Samuel;					
**CONTINUING DATA VERIFIED: THIS APPLN CLAIMS BENEFIT OF 60/272,237 02/27/2001 <i>YJS AR 10/30/02</i>					
<h1>BEST AVAILABLE COPY</h1>					
** FOREIGN APPLICATIONS VERIFIED: <i>n AR 10/30/02</i>					
PG-PUB DO NOT PUBLISH <input type="checkbox"/>		RESCIND <input type="checkbox"/>			
Foreign priority claimed <input type="checkbox"/> yes <input checked="" type="checkbox"/> no		ATTORNEY DOCKET NO			
35 USC 119 conditions met <input type="checkbox"/> yes <input checked="" type="checkbox"/> no		CPAC 1008-2 US			
Verified and Acknowledged Examiners's initials <i>AR 10/30/02</i>					
TITLE : Chip scale package with flip chip interconnect					

U.S. DEPT. OF COMM./PAT. & TM-PTO-436L (Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G.
Assistant Examiner			
ISSUE FEE		DRAWING	
Amount Due	Date Paid	Sheets Drwg.	Figs. Drwg.
			Print Fig.
<input type="checkbox"/> TERMINAL DISCLAIMER		Primary Examiner	
		Applicati n Examiner	
PREPARED FOR ISSUE			
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